I CLAIM:

1. A process for correcting a resampler (6) with which a sampled input signal (S_D), which is subjected to an input sampling rate (f_A) and which has one of symbol and chip frequencies (f_C) that deviates from the input sampling rate (f_A), is converted to a sampled output signal (S_C), for which an output sampling rate corresponds with the one of the symbol and chip frequencies by changing the input sampling rate (f_A) by a resampling factor (resamp_fac), the process including the following process steps:

performing (8) a non-linear operation on the input signal (S_D), so that a spectral line (15) arises at the one of the symbol and chip frequencies;

spectrally shifting (9) the input signal (S_D) by the one of the symbol and chip frequencies (f_C);

determining (11) the phase (φ) of the shifted spectral line (15) at the one of the symbol and chip frequencies (f_C) as a function of the sample time points; and

correcting one of the resampling factor (resamp_fac) and a time shift of the output signal (S_C) by a time correction value (resamp_offset) based on a regression of the phase (φ) of the shifted spectral line (15) at the one of the symbol and chip frequencies (f_C) as a function of the sample time points.

2. The process of claim 1, wherein the non-linear operation is a squaring.

3. The process of claim 1, wherein the linear regression of the phase (φ) of the shifted spectral line (15) at the symbol or chip frequency (S_C) is performed as a function of the sample time points.

4. The process of claim 3, wherein the linear regression produces a compensation straight line (17);

wherein the resampling factor (resamp_fac) is corrected on the basis of a slope ($\Delta\varphi$) of the compensation straight line (17); and

wherein the time correction value (resamp_offset) is corrected on the basis of an axis (φ_0) defining the compensation straight line (17).

5. The process of claim 1, wherein before the phase (φ) is determined a decimation (10) of the sampling value is performed by a preceding band limitation.

6. The process of claim 5, wherein the decimation (10) of the sampling value is performed by a filter whose frequency response has zero positions at at least the one of the symbol and chip frequencies (f_C) and at double the at least one of the symbol and chip frequencies ($2f_C$).

7. An apparatus (2) for correcting a resampler (6) in which a sampled input signal (S_D), which has been subjected to an input

sampling rate and which has one of symbol and chip frequencies (f_C) which deviates from the input sampling rate, is converted into a sampled output signal (S_C), for which the sampling rate corresponds to the one of the symbol and chip frequencies (f_C), by changing the input sampling rate (f_A) by a resampling factor (resamp_fac), comprising:

a non-linear operating element (8) that subjects the input signal (S_D) to a non-linear operation so that a spectral line (15) results at the one of the symbol and chip frequencies (f_C);

a frequency shifter (9), which spectrally shifts the input signal (S_D) by the one of the symbols and chip frequencies (f_C);

a phase determining device (11) that determines the phase (φ) of the shifted spectral line (15) at the one of the symbol and chip frequencies (f_C) as a function of the sampling time points; and

a regression and correcting device (13) that, on the basis of a regression of the phase (φ) of the shifted spectral line (15) at the one of the symbol and chip frequencies (f_C), performs one of: correcting the resampling factor (resamp_fac) as a function of the sample time points and time-wise shifting the output signal (S_C) by a time correction value (resamp_offset).

8. The apparatus of claim 7, wherein the non-linear operating element (8) is a squarer.

9. The apparatus of claim 7, wherein a decimating device (10) is provided between the frequency shifter (9) and the phase determining device (11) in which a decimation of the sampling value is performed by sub-sampling with a preceding band limitation.

10. The apparatus of claim 9, wherein the decimating device (10) includes a filter whose frequency response has zero positions at the one of the symbol and chip frequencies (f_c) and double the one of the symbol and chip frequencies ($2f_c$).